Principles of Semiconductor Devices

(집적 회로 소자)

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Circuit Modeling & Simulation
Circuit Modeling

- Demands of Industrial Circuit Design & Circuit Simulation

  ✓ The need to properly account for
    • The behavior of the device characteristics has lead to model
    • Methods of dealing with process variability
    • Formulation of the model equations implies that certain types of data must be made available for parameter extraction

  ✓ Rather than employing an iterative succession of breadboarding and testing of designs

  ✓ A circuit would be designed, evaluated, and redesigned using only computer simulation.
Philosophy for Models Suitable for Analog Design

The model required for analog design with CMOS technology is one that leads to understanding and insight as distinguished from accuracy.

This chapter is devoted to the simple model suitable for design not using simulation.
The Analog IC Design Flow

- Conception of the idea
- Definition of the design
- Implementation
- Comparison with design specifications
- Simulation
- Physical Definition
- Physical Verification
- Parasitic Extraction
- Fabrication
- Testing and Verification
- Product
Circuit Modeling

- **SPICE**: Simulation Program with Integrated Circuit Emphasis

  - University of California, Berkeley in the late 1960s
  - Any circuit is treated in a node/element fashion → can be thought of as the main program
  - Element models are subroutines that are called when the behavior of an element must be evaluated

- ✔ SPICE (UC Berkeley)
- ✔ HSPICE (Meta – Software, Inc.)
- ✔ PSPICE (for Personal use)
- ✔ SSPICE (Silvaco)
Circuit Modeling

- **SPICE**: Simulation Program with Integrated Circuit Emphasis

  ✓ The use of SPICE to simulate Integrated Circuits,
    - 1\textsuperscript{st} level: basic methods of using SPICE to simulate various circuits
    - 2\textsuperscript{nd} level: a variety of issues revolving around the mathematical and numerical methods involved in simulating circuits
      → where the focus is on ensuring the convergence of the simulation while making efficient use of computing resources
    - 3\textsuperscript{rd} level: element models used to describe MOSFETs

  ✓ To make effective use of the FET models available in SPICE,
    → User must understand the construction and implementation of those models
Circuit Modeling

- Modeling in SPICE:

  - Current – Voltage characteristics of the FET
  - The Capacitance – Voltage characteristics of the FET
    - Described by a small set of rather simple equation, with a few parameters to match the model to the specific silicon technology
    - Determined by very simple parameter extraction, using a linear least squares method
Circuit Modeling

Modeling in SPICE:

- As FET technology has evolved the situation has become a good deal more complex.
  - Lead to an increasing number of model parameters
  - Effect of increasingly shifting the burden of modeling the FET from the model equation formulation to the process of extracting the model parameters
  - Those more complicated model equations have forced the use of non linear least squares curve – fitting techniques, which are numerical and iterative

Model Parameters
- Physical Parameters: treated as having direct and quantifiable physical meaning
  - (ex) Gate oxide thickness
- Electrical Parameters: defined from parameter extraction, and thus may actually have little direct physical meaning
  - (ex) Junction depth

- When a large number of electrical parameters must be determined, Parameter extraction grows to assume a very large degree of importance
Circuit Modeling

SPICE 개요

- SPICE (Simulation Program with Integrated Circuit Emphasis)
- 1970년대 U.C. Berkeley에서 개발
- 정확한 회로 시뮬레이션 결과를 얻기 위해서 device model을 정확하게 명시하는 것이 필요
- MNA(Modified Nodal Analysis) 회로 해석 방식 사용
- 회로동작에 대한 feeling(감)과 SPICE simulation 결과의 validity 판정을 위해 hand analysis가 필수적임
Circuit Modeling

SPICE 입력 및 출력파일 형태

• SPICE 입력 파일
  - title line
  - 회로 소자 및 연결
  - 해석 방식 ( .DC, .TRAN, .AC, .OP, .NOISE 등)
  - 출력 방식 ( .PRINT, .PLOT 등)
  - 소자의 모델 파라미터
  - .END

• SPICE 출력 파일
  - 각 노드 전압
  - 전압원, 인덕터와 controlled voltage source의 전류
Circuit Modeling

SPICE 입력 file의 예

- Diode 회로

DIODE Rectifier Circuit

DX 1 2 DMOD
R1 2 0 10K
VIN 1 0 DC 0
.MODEL DMOD D IS=1E-15 N=1.5
*COMMENT LINE
.DC VIN -5 5 0.1
.PRINT DC V(1) V(2) I(VIN)
.END
Circuit Modeling

SPICE 회로 해석 방법

- MNA(modified nodal analysis) 방식을 채택
- Nodal analysis 방식
  - 회로의 각 node에서 KCL을 적용하여 각 node 전압 계산
  - voltage source, inductor, controlled voltage source가 있을 경우 회로 방정식이 풀리지 않음
- MNA(Modified Nodal Analysis) 방식이라?
  - 각 node에 KCL 적용
  - voltage source, inductor, controlled voltage source: KVL 적용
Circuit Modeling

SPICE 회로 해석 방법

• Nodal Analysis 해석 예

• 변수: 노드 전압: V1, V2

\[
\begin{align*}
\frac{1}{R_1} \cdot V_1 - \frac{1}{R_2} \cdot V_2 &= I_s \\
-\frac{1}{R_1} \cdot V_1 + \left(\frac{1}{R_1} + \frac{1}{R_2}\right) \cdot V_2 &= 0
\end{align*}
\]

⇒ V1, V2
SPICE 회로 해석 방법

• MNA 방식 해석 예
• 변수: 노드전압(V1, V2), 전압원 전류(Iv)

\[
\begin{align*}
\frac{1}{R_1} \cdot V_1 - \frac{1}{R_1} \cdot V_2 + I_V &= 0 \\
- \frac{1}{R_1} \cdot V_1 + \left( \frac{1}{R_1} + \frac{1}{R_2} \right) \cdot V_2 &= 0 \\
V_1 &= V_{in} \\
\Rightarrow \quad V_1, V_2, I_V
\end{align*}
\]
SPICE 회로 해석

- MNA 방식 해석 예 2
- 변수: 노드 전압($V_1, V_2$), 전압원 전류($I_{in}$)
- I-V 특성이 비선형 소자의 경우에는 반복법 사용

\[
\begin{align*}
    f_1(V_1, V_2, I_{in}) &= I_s \cdot \left( e^{\frac{V_1 - V_2}{nV_T}} - 1 \right) + I_{in} = 0 \\
    f_2(V_1, V_2, I_{in}) &= -I_s \cdot \left( e^{\frac{V_1 - V_2}{nV_T}} - 1 \right) + \frac{V_2}{R} = 0 \\
    f_3(V_1, V_2, I_{in}) &= V_1 - V_{in} = 0
\end{align*}
\]

3차원 비선형 방정식
뉴턴 래프슨 반복법 (Newton Raphson iteration)

1) 직선식 \[ f'(x^m) \cdot (x - x^m) + f(x^m) = 0 \]

2) \[ x^{m+1} = x^m - \frac{f(x^m)}{f'(x^m)} \]

1차원 비선형 방정식 \[ f'(x^m) \cdot (x - x^m) = -f(x^m) \]
Newton-Raphson Iteration

- Front diode circuit with 3-terminal circuit is obtained by changing the circuit.
- Recalculate until convergence.
- Uplift the basic function in the basic function and have a possibility of yield.

Initial circuit function\[ f'(x^m) \cdot (x - x^m) = - f(x^m) \]

\[
\begin{bmatrix}
\frac{\partial f_1}{\partial V_1} & \frac{\partial f_1}{\partial V_2} & \frac{\partial f_1}{\partial I_{in}} \\
\frac{\partial f_2}{\partial V_1} & \frac{\partial f_2}{\partial V_2} & \frac{\partial f_2}{\partial I_{in}} \\
\frac{\partial f_3}{\partial V_1} & \frac{\partial f_3}{\partial V_2} & \frac{\partial f_3}{\partial I_{in}}
\end{bmatrix}
\begin{bmatrix}
V_1^{m+1} - V_1^m \\
V_2^{m+1} - V_2^m \\
I_{in}^{m+1} - I_{in}^m
\end{bmatrix}
= \begin{bmatrix}
-f_1(V_1^m, V_2^m, I_{in}^m) \\
-f_2(V_1^m, V_2^m, I_{in}^m) \\
-f_3(V_1^m, V_2^m, I_{in}^m)
\end{bmatrix}

at\ V_1^m, V_2^m, V_3^m
Diode 회로의 3차원 비선형 방정식

\[ f_1(V_1, V_2, I_{in}) = I_S \cdot \left(e^{\frac{V_1 - V_2}{nV_T}} - 1\right) + I_{in} = 0 \]

\[ f_2(V_1, V_2, I_{in}) = -I_S \cdot \left(e^{\frac{V_1 - V_2}{nV_T}} - 1\right) + \frac{V_2}{R} = 0 \]

\[ f_3(V_1, V_2, I_{in}) = V_1 - V_{in} = 0 \]
디오드 회로 3차원 비선형 방정식의 선형화

일차원 비선형방정식  \( f'(x^m) \cdot x = -f(x^m) + f'(x^m) \cdot x^m \)

\[
\begin{bmatrix}
geq_m & -\geq_m & 1 \\
-\geq_m & \geq_m & 0 \\
1 & 0 & 0 \\
\end{bmatrix}
\begin{bmatrix}
V_1^{m+1} \\
V_2^{m+1} \\
I_{in}^{m+1} \\
\end{bmatrix}
= 
\begin{bmatrix}
-I_D^m + \geq_m \cdot V_D^m \\
I_D^m - \geq_m \cdot V_D^m \\
V_{in} \\
\end{bmatrix}
\]

이기서
\( I_D^m = I_S \cdot (e^{\frac{V_D^m}{nV_T}} - 1) \)
\( V_D^m = V_1^m - V_2^m \)
\( \geq_m = \frac{\partial I_D}{\partial V_D} \bigg|_{V_D = V_D^m} = \frac{I_S}{nV_T} \cdot e^{\frac{V_D^m}{nV_T}} \)
뉴턴 랩슨 반복법 (Newton Raphson iteration)

• Convergence 판정 routine

1) 각 비선형 소자 (Diode, BJT, MOSFET, JFET 등)들의 DC 전류
   들의 convergence check를 행함.
   예: MOSFET 드레인 전류 (별크 전류에 대해서도 같은 과정을 반복함)
   
   \[ |cd_{\text{hat}} - cd| \leq ABSTOL + RELTOL \times \max (|cd_{\text{hat}}|, |cd|) \]

   cd : drain 전류 값 (DC 값)
   cd_{\text{hat}} : 지난 번 iteration 때의 drain 전류값과 conductance 값들 (gm, gds, gmbs)로부터 예측된 drain 전류 값

2) 모든 node 전압 및 voltage source와 inductor와 dependent voltage source의 전류들에 대한 convergence test를 행한다.
• Convergence 제어 파라미터 들

*node 전압 convergence: VNTOL, RELTOL 파라미터들을 사용

*전류 convergence: ABSTOL, RELTOL 파라미터들을 사용

*HSPICE : ABSI, RELI, ABSV, RELV 등의 파라미터들을 사용
What’s modeling?

- Process Device
- Design

Real World | Simulated World

Bridge or Information Set

All about Devices
- DC
- AC
- Worst Case
- Reliability
- etc
What’s the Device Model Parameter?

- **Key Word**
  - Model(Equation): \( I_{ds} = f(V_{ds}, V_{gs}, V_{bs}, \ldots \text{etc}) \)
    \[ = A \times V_{ds} + B \times V_{gs} + C \times V_{bs} + D \]
  - Model Parameter: \( A, B, C, D \)

MOSFET Model History

- **1st Gen.**
  - BSIM1
  - BSIM2
  - BSIM3
  - BSIM4
  - HYSIM

- **2nd Gen.**
  - Level=28 (MBSIM)

- **3rd Gen.**
  - Physical Model
    - Upgrade(Unified Model)
      - Continuous
      - Accurate
      - Physical Model
  - Bias Dependence
    - Accurate
    - Non-Convergence
    - Non-Physical
  - Inverse Geometry Dependence
    - Accurate
    - Non-Convergence
    - Non-Physical

- **Process/Device Development**
- **MOSFET Model Setup & Parameter Extraction**
- **Circuit Design & Simulation**
Summary of the Simple Large Signal MOSFET Model

N-channel reference convention:

Non-saturation-

\[
i_D = \frac{W\mu_0 C_{ox}}{L} \left[ (v_{GS} - V_T)v_{DS} - \frac{v_{DS}^2}{2} \right] (1 + \lambda v_{DS})
\]

Saturation-

\[
i_D = \frac{W\mu_0 C_{ox}}{L} \left[ (v_{GS} - V_T)v_{DS(sat)} - \frac{v_{DS(sat)}^2}{2} \right] (1 + \lambda v_{DS}) = \frac{W\mu_0 C_{ox}}{2L} (v_{GS} - V_T)^2 (1 + \lambda v_{DS})
\]

where:

- \(\mu_0\) = zero field mobility (cm²/volt·sec)
- \(C_{ox}\) = gate oxide capacitance per unit area (F/cm²)
- \(\lambda\) = channel-length modulation parameter (volts⁻¹)
- \(V_T = V_{T0} + \gamma(\sqrt{2|\phi_f| + |V_{BS}|} - \sqrt{2|\phi_f|})\)
- \(V_{T0}\) = zero bias threshold voltage
- \(\gamma\) = bulk threshold parameter (volts⁻⁰₅)
- \(2|\phi_f|\) = strong inversion surface potential (volts)

For p-channel MOSFETs, use n-channel equations with p-channel parameters and invert current.
# MOSFET Parameters

Model Parameters for a Typical CMOS Bulk Process (0.8μm CMOS n-well):

<table>
<thead>
<tr>
<th>Parameter Symbol</th>
<th>Parameter Description</th>
<th>Typical Parameter Value</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{T0} )</td>
<td>Threshold Voltage ( (V_{BS} = 0) )</td>
<td>( 0.7 \pm 0.15 )</td>
<td>( -0.7 \pm 0.15 )</td>
</tr>
<tr>
<td>( K' )</td>
<td>Transconductance Parameter (in saturation)</td>
<td>( 110.0 \pm 10% )</td>
<td>( 50.0 \pm 10% )</td>
</tr>
<tr>
<td>( \gamma )</td>
<td>Bulk threshold parameter</td>
<td>0.4</td>
<td>0.57</td>
</tr>
<tr>
<td>( \lambda )</td>
<td>Channel length modulation parameter</td>
<td>( 0.04 \ (L=1 \mu m) )</td>
<td>( 0.05 \ (L=1 \mu m) )</td>
</tr>
<tr>
<td>( 2\phi_F )</td>
<td>Surface potential at strong inversion</td>
<td>0.7</td>
<td>0.8</td>
</tr>
</tbody>
</table>
3.4 - CAPACITANCES OF THE MOSFET

Types of Capacitance
Physical Picture:

MOSFET capacitors consist of:
- Depletion capacitances
- Charge storage or parallel plate capacitances
Circuit Modeling

MOSFET Depletion Capacitors

Model:
1.) \( v_{BS} \leq FC \cdot PB \)

\[
C_{BS} = \frac{CJ \cdot AS}{1 - \frac{v_{BS}}{PB}} + \frac{CJSW \cdot PS}{1 - \frac{v_{BS}}{PB}} \cdot \frac{MJSW}{MJ} ,
\]

and

2.) \( v_{BS} > FC \cdot PB \)

\[
C_{BS} = \frac{CJ \cdot AS}{1 - FC} \left( 1 - (1 + MJ)FC + MJ \frac{V_{BS}}{PB} \right) + \frac{CJSW \cdot PS}{1 + MJSW} \left( 1 - (1 + MJSW)FC + MJSW \frac{V_{BS}}{PB} \right)
\]

where
- \( AS \) = area of the source
- \( PS \) = perimeter of the source
- \( CJSW \) = zero bias, bulk source sidewall capacitance
- \( MJSW \) = bulk-source sidewall grading coefficient

For the bulk-drain depletion capacitance replace "S" by "D" in the above.
Circuit Modeling

Charge Storage (Parallel Plate) MOSFET Capacitances - $C_1, C_2, C_3$ and $C_4$

Overlap capacitances:

$$C_1 = C_3 = L_D \cdot W_{\text{eff}} \cdot C_{\text{ox}} = \text{CGSO or CGDO}$$

($L_D \approx 0.015$ μm for LDD structures)

Channel capacitances:

$$C_2 = \text{gate-to-channel} = C_{\text{ox}}W_{\text{eff}}(L-2L_D) = C_{\text{ox}}W_{\text{eff}}L_{\text{eff}}$$

$$C_4 = \text{voltage dependent channel-bulk/substrate capacitance}$$
Circuit Modeling

Charge Storage (Parallel Plate) MOSFET Capacitances - $C_5$

View looking down the channel from source to drain

$C_5 = CGBO$

Capacitance values based on an oxide thickness of 140 Å or $C_{ox} = 24.7 \times 10^{-4}$ F/m²:

<table>
<thead>
<tr>
<th>Type</th>
<th>P-Channel</th>
<th>N-Channel</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>CGSO</td>
<td>$220 \times 10^{-12}$</td>
<td>$220 \times 10^{-12}$</td>
<td>F/m</td>
</tr>
<tr>
<td>CGDO</td>
<td>$220 \times 10^{-12}$</td>
<td>$220 \times 10^{-12}$</td>
<td>F/m</td>
</tr>
<tr>
<td>CGBO</td>
<td>$700 \times 10^{-12}$</td>
<td>$700 \times 10^{-12}$</td>
<td>F/m</td>
</tr>
<tr>
<td>CJ</td>
<td>$560 \times 10^{-6}$</td>
<td>$770 \times 10^{-6}$</td>
<td>F/m²</td>
</tr>
<tr>
<td>CJSW</td>
<td>$350 \times 10^{-12}$</td>
<td>$380 \times 10^{-12}$</td>
<td>F/m</td>
</tr>
<tr>
<td>MJ</td>
<td>0.5</td>
<td>0.5</td>
<td></td>
</tr>
<tr>
<td>MJSW</td>
<td>0.35</td>
<td>0.38</td>
<td></td>
</tr>
</tbody>
</table>
Contents

- MOS modeling 구성
- Modeling 추세 및 방향
- Specific device 모델링
  - TFT (Thin Film Transistor) 모델링
  - SOI (Silicon-On-Insulator) 모델링
  - HVMOS (High Voltage MOS) 모델링
Circuit Modeling

MOS Modeling

- Convergence issue
  - Discontinuity (piece-wise conjunction)
  - Negative conductance

- Speed issue
  - Compact Modeling (equation/modeling)
  - Continuous characteristics
Circuit Modeling

MOS Sub-modeling

- Modeling 구분

HSPICE 모델링 방법

- Drain current
- Gate capacitance
- Junction Diode
- Series Resistance
- Temperature
- Impact Ionization
- Worst-case (Process skew)
- Binning methods
- Automatic model Selection
Historical Evolution of MOS model

- MOS model
  - DSM에서 복잡한 physics를 나타냄
  - Physical model의 필요성이 증가함

![Graph showing the historical evolution of MOS models over the years.](image-url)
Model History

- **First Generation Models**
  - Level 1, 2, 3
    - Simple and Physically Based Model
    - Analytical description rather than behavior of model equations in circuit simulator
    - Inefficient for Circuit Simulations

- **Second Generation Models**
  - BSIM, BSIM2, Level 28 (Modified BSIM)
    - Complex and many Empirical M/P based Model
    - Mathematically Conditioned for Efficient Circuit Simulation
    - Polynomial Functions
    - More Accurate Fitting to measured data, But weaken link between M/P and fabrication process
Model History

• Third Generation Models
  – BSIM3, MOS model 9, EKV Model, PCIM Model
    • Return to Physically Based Model (Reduction of Number of M/P)
    • Well-behaved Smoothing Function
    • Continuous and Single Unified Model Current Equations
  – BSIM4
  – BSIM5

- MOS Model 9: Philips Electronics Laboratory
- EKV Model: Swiss Federal Institute of Technology in Lausanne
- PCIM Model: Digital Equipment Corporation
Circuit Modeling

**JFET Models**
- Level=1: Schichman and Hodges
- Level=2: Improvement of UCB

**VCSEL Diode Models**
- Level=4: New RPI VCSEL Diode

**Ferrocap Models**
- Level=5: FCAP Model
- Level=6: FRMC Model

**TFT Models**
- Level = 15: Modified Leroux (Armorphous TFT Model)
- Level= 16: Modified UCB Model (Poly TFT Model)

**VERSION=1**

**VERSION=2**

**VERSION=2**
- SCALERPI=1
- LU1, LMS, LU0
- CT, L0, Smart=3
First Generation Model I

• **Level 1**

  ✓ Gradual Channel Approximation
  \[
  \frac{d^2 \phi}{dx^2} + \frac{d^2 \phi}{dy^2} \sim \frac{d^2 \phi}{dx^2} = -\frac{\rho(x)}{\varepsilon_{si}}
  \]

  ✓ Square Law for Saturation Current
  \[
  I_{ds} = \frac{\mu C_{ox} W}{L} [V_{gs} - V_{th} - 0.5V_{ds}]V_{ds}
  \]

  ✓ $\lambda$-model for Channel Length Modulation (Rout is a single value.)
  \[
  I_{ds} = I_{dsat}[1 + \lambda V_{ds}]
  \]

  ✓ No Sub-threshold Conduction Model
First Generation Model II

• Level 2
  ✓ First attempt for Small Geometry Effects
  ✓ Charge Sharing and Narrow Width Effect
  ✓ Mobility Reduction by Vertical field
  ✓ No DIBL and Mobility Reduction by Lateral field
  ✓ $I_{ds}$ has $3/2$ power term. ($G_{ds}$ is discontinuous around $V_{dsat}$)
  ✓ Sub-threshold Current Model ($G_{m}$ is discontinuous around $V_{th}$)
  ✓ Slow, Inefficient, and Convergence Problems
First Generation Model III

• Level 3
  ✓ Drain Induced Barrier Lowering Effect in Threshold Voltage
  ✓ Mobility Reduction by Lateral Field
  ✓ No 3/2 Power term in Ids [Taylor Expansion]
  ✓ Sub-threshold Conduction model in Level 2.
  ✓ Discontinuity of Gds and Gm at Vdsat and Vth.
  ✓ Digital Circuit
Second Generation Model

• BSIM (Berkeley Short-Channel IGFET Model)
  ✔ Mathematical Emphasis for Circuit Simulation
  ✔ Strictly Empirical Model for Small Geometry
  ✔ Improved Vth model (expanded to non-uniformly doped substrates)
  ✔ Mobility Model
  ✔ Polynomial Model for Ids
  ✔ Vdsat (Velocity Saturation Effect is included.)
  ✔ Sub-threshold Current Model (Ids=Ids,weak + Ids, strong)
  ✔ Negative Conductance in certain conditions
Second Generation Model

• Level 28
  ✓ Modified BSIM Model (Meta-Software)
  ✓ Designed to accommodate Binning (Continuous across Bin Boundary)
  ✓ Vdsat region is well-behaved. (Additional Sub-regions)
  ✓ Sub-threshold region is well-behaved. (Additional Sub-regions)
  ✓ M/P set is almost entirely Empirical.
  ✓ Digital and Analog Circuit Simulation

• BSIM 2
  ✓ Modified Vth model (No negative conductance)
  ✓ Mobility Model (New quadratic term for higher vertical field)
  ✓ No Negative Output Conductance
  ✓ Sub-threshold region is well-behaved.
  ✓ Digital and Analog Circuit
## Circuit Modeling

<table>
<thead>
<tr>
<th>특징 \ 모델</th>
<th>BSIM1</th>
<th>Level 28</th>
<th>BSIM2</th>
<th>BSIM3v3</th>
<th>BSIM4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Public (HSPICE level)</td>
<td>Public (13)</td>
<td>HSPICE only (28)</td>
<td>Public (39)</td>
<td>Public (49)</td>
<td>Public</td>
</tr>
<tr>
<td>Application</td>
<td>Digital</td>
<td>Digital</td>
<td>Analog/Digital</td>
<td>Analog/Digital</td>
<td>Analog/Digital</td>
</tr>
<tr>
<td>Gds &gt;0</td>
<td>No</td>
<td>Yes</td>
<td>No</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>미분값 연속성</td>
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<td>Transition 부분 연속성 우수</td>
<td>Single I-V mode</td>
<td>RF model 강화</td>
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<td>Negative Gds</td>
<td>BSIM 문제 개선</td>
<td>Compact 모델</td>
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<td>Pocket/delta dop. Vth</td>
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<td>Transition 부분 연속성 우수</td>
<td>Product param</td>
<td>Conductance / Current</td>
<td>Improved 1/f noise</td>
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# MOSFET Model Comparison V

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<th>BSIM2</th>
<th>BSIM3 v2</th>
<th>BSIM3 v3</th>
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## Summary

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<tr>
<th>Model</th>
<th>BSIM3 v3.2</th>
<th>LEVEL 28</th>
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<tr>
<td>Physically Base Model</td>
<td>Physically Base Model</td>
<td>Empirical Model</td>
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<td>Binning</td>
<td>Global 1set Model (Binning)</td>
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<td>Vth Model</td>
<td>Quasi 2D Analysis</td>
<td>Body Effect</td>
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<td>Body Effect, SCE, RSCE, NWE, DIBL</td>
<td>Body Effect, DIBL</td>
<td>Vertical and Lateral Field</td>
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<td>Mobility Model</td>
<td>Mobility Reduction</td>
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<td>Vertical and Lateral Field</td>
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<td>Rout Model</td>
<td>CLM, DIBL, SCBE</td>
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<td>Poly Depletion Effect</td>
<td>Considered</td>
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<td>Transition</td>
<td>Vdseff for Unified Vds around Vdsat</td>
<td>Three Sub-Regions</td>
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<td>Vgseff for Unified Vgs around Vth</td>
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<td>DC parameter</td>
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<td>Charge Thickness Model</td>
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BSIM3v3 모델

- 기본 전류방정식의 유도
- 소스 드레인 직렬 저항 효과
- 이동도
- Bulk depletion 전하식의 선형화
- Threshold 전압(VTH) 식
- DIBL 현상
- Threshold 전압의 short channel 효과
- Threshold 전압의 narrow channel 효과
- Channel length modulation 효과
- Saturation 영역 전류식
- substrate 전류와 subthreshold 전류
- 노이즈 모델과 온도의존성 모델
BSIM3 모델의 특징

- 모델방정식에 채널 길이 $L$과 채널 폭 $W$ 의존 성을 많이 추가함으로써, 한 칩의 설계에 사용 되는 모든 $L$과 $W$ 범위에 대해 NMOS와 PMOS 각각 한 개의 모델 파라미터 세트만 사용한다
Circuit Modeling

MOSFET

General form

M<name> <drain node> <gate node> <source node>
+ <bulk/substrate node> <model name>
+ [L=<value>] [W=<value>]
+ [AD=<value>] [AS=<value>]
+ [PD=<value>] [PS=<value>]
+ [NRD=<value>] [NRS=<value>]
+ [NRG=<value>] [NRR=<value>]
+ [M=<value>] [N=<value>]

Examples

M1 14 2 13 0 PNMOM L=25u W=12u
M13 15 3 0 0 PSTRONG
M16 17 3 0 0 PSTRONG M=2
M28 0 2 100 100 NWEAK L=33u W=12u
+ AD=288p AS=288p PD=60u PS=60u NRD=14 NRS=24 NRG=10

Model form

.MODEL <model name> NMOS [model parameters]
.MODEL <model name> PMOS [model parameters]

Description

The MOSFET is modeled as an intrinsic MOSFET using ohmic resistances in series with the drain, source, gate, and bulk (substrate). There is also a shunt resistance (RDS) in parallel with the drain-source channel.
The simulator provides six MOSFET device models, which differ in the formulation of the I-V characteristic. The LEVEL parameter selects among different models as shown below. For more information, see References.

- LEVEL=1  Shichman-Hodges model (see reference [1])
- LEVEL=2  geometry-based, analytic model (see reference [2])
- LEVEL=3  semi-empirical, short-channel model (see reference [2])
- LEVEL=4  BSIM model (see reference [3])
- LEVEL=5  EKV model version 2.6 (see reference [10])
- LEVEL=6  BSIM3 model version 2.0 (see reference [7])
- LEVEL=7  BSIM3 model version 3.1 (see reference [8])
Model level 5 (EKV version 2.6)

The EKV model is a scalable and compact model built on fundamental physical properties of the device. Use this model to design low-voltage, low-current analog, and mixed analog-digital circuits that use sub-micron technologies. The charge-based static, quasi-static dynamic, and noise models are all derived from the normalized transconductance-to-current ratio, which is accurately described for all levels of current, including the moderate inversion region. A single I-V expression preserves the continuity of first- and higher-order derivatives with respect to any terminal voltage in all regions of device operation.

Version 2.6 models the following:

- geometrical and process related aspects of the device (oxide thickness, junction depth, effective channel length and width, and so on)
- effects of doping profile and substrate effects
- weak, moderate, and strong inversion behavior
- mobility effects due to vertical and lateral fields and carrier velocity saturation
- short-channel effects such as channel-length modulation, source and drain charge sharing, and the reverse short channel effect
- thermal and flicker noise modeling
- short-distance geometry and bias-dependent device matching for Monte Carlo analysis.
Model levels 1, 2, and 3

The DC characteristics of the first three model levels are defined by the parameters VTO, KP, LAMBDA, PHI, and GAMMA. These are computed by the simulator if process parameters (e.g., TOX, and NSUB) are given, but the user-specified values always override. VTO is positive (negative) for enhancement mode and negative (positive) for depletion mode of N-channel (P-channel) devices.

The default value for TOX is 0.1 μ for Levels 2 and 3, but is unspecified for Level 1, which discontinues the use of process parameters.

For MOSFETs the capacitance model has been changed to conserve charge, affecting only the Level 1, 2, and 3 models.

Effective length and width for device parameters are calculated with the formula:

\[ P_i = P_o + P_e/L_e + P_w/W_e \]

where:

\[ L_e = \text{effective length} = L - (L_D \cdot 2) \]
\[ W_e = \text{effective width} = W - (W_D \cdot 2) \]
Model level 4

Unlike the other models in PSpice, the BSIM model is designed for use with a process characterization system that provides all parameters. Therefore, there are no defaults specified for the parameters, and leaving one out can cause problems.

The LEVEL=4 (BSIM1) model parameters are all values obtained from process characterization, and can be generated automatically. Reference [4] of References describes a means of generating a process file, which must then be converted into MODEL (model definition) statements for inclusion in the Model Library or circuit file. (The simulator does not read process files.)

The level 4 (BSIM) and level 6 (BSIM3 version 2) models have their own capacitance model, which conserves charge and remains unchanged. References [6] and [7] describe the equations for the capacitance due to channel charge.

In the following MOSFET model parameters list, parameters marked with a $\zeta$ in the Default column also have corresponding parameters with a length and width dependency. For example, VFB is a basic parameter using units of volts, and LVFB and WVFB also exist and have units of volt $\mu$. The formula

$$P_{\zeta} = P_{v} + P_{c}/L_{x} + P_{w}/W_{x}$$

is used to evaluate the parameter for the actual device, where:

$$L_{x} = \text{effective length} = L - DL$$

$$W_{x} = \text{effective width} = W - DW$$
Circuit Modeling

Model level 6 (BSIM3 version 2.0)

The Level 6 Advanced parameters should not be changed unless the detail structure of the device is known and has specific, meaningful values.

The BSIM3 model is a physical model using extensive built-in dependencies of important dimensional and processing parameters. It includes the major effects that are important to modeling deep-submicrometer MOSFETs, such as threshold voltage reduction, nonuniform doping, mobility reduction due to the vertical field, bulk charge effect, carrier velocity saturation, drain-induced barrier lowering (DIBL), channel length modulation (CLM), hot-carrier-induced output resistance reduction, subthreshold conduction, source-drain parasitic resistance, substrate current induced body effect (SCBE), and drain voltage reduction in LDD structure. For additional, detailed model information, see References.

Additional notes

Note 1  If any of the following BSIM3 version 2.0 model parameters are not explicitly specified, they are calculated using the following equations.

\[ V_{TH0} = V_{FB} + \Phi + K_1 \Phi \]
\[ K_1 = \text{GAMMA2} - 2 \cdot K_2 \cdot (\Phi - V_{BM}) \]
\[ K_2 = \frac{(\text{GAMMA1} - \text{GAMMA2}) \cdot (\Phi - V_{BX} - \Phi_0)}{2 \cdot \Phi (\Phi - V_{BX} - \Phi_0 - V_{BM})} \]
\[ V_{FB} = V_{TH0} - K_1 \cdot \Phi \]
\[ \Phi = \sqrt{2 \left( \frac{e \Phi_{NPEAK}}{n_i} \right)} \]
\[ \text{GAMMA1} = \frac{\sqrt{2 q e_i N_{PEAK}}}{\text{COX}} \]
\[ \text{GAMMA2} = \frac{\sqrt{2 q e_i N_{SUB}}}{\text{COX}} \]
\[ V_{BX} = \Phi - q \cdot N_{PEAK} \cdot X T^2 / (2 \varepsilon_{ox}) \]
\[ L_{ITL} = \frac{e_{ox} Y_{OX}}{e_{ox}} \]

H. S. Yoon
Model level 7 (BSIM3 version 3.1)

The BSIM3 version 3.1 model was developed by the University of California, Berkeley, as a deep submicron MOSFET model with the same physical basis as the BSIM3 version 2 model, but with a number of major enhancements, such as a single I-V expression to describe current and output conductance in all regions of device operation, better modeling of narrow width devices, a reformulated capacitance model to improve short and narrow geometry models, a new relaxation time model to improve transient modeling, and improved model fitting of various W/L ratios using one parameter set. BSIM3 version 3.1 retains the extensive built-in dependencies of dimensional and processing parameters of BSIM3 version 2. For additional, detailed model information, see Reference [8] of References.
Circuit Modeling

Additional notes

**Note 1**  If any of the following BSIM3 version 3.1 model parameters are not explicitly specified, they are calculated using the following equations:

If $V_{THO}$ is not specified, then:

$$V_{THO} = V_{FB} + \Phi_i K1 \sqrt{\Phi_i}$$

where:

$$V_{FB} = -1.0$$

If $V_{THO}$ is specified, then:

$$V_{FB} = V_{THO} - \Phi_i + K1 \sqrt{\Phi_i}$$

$$V_{BX} = \frac{\Phi_i - 0.9 \cdot NCH \cdot XT^2}{2 \cdot \epsilon_{Si}}$$

$$CF = \left(\frac{2e_{ox}}{\pi}\right) \left(1 + 4 \times 10^{-7} \frac{T}{TOX}\right)$$

where

$$E_g(T) = \text{the energy bandgap at temperature } T = 1.16 - \left(7.02 \cdot 10^{-4} \cdot \frac{T^2}{T + 1108}\right)$$

**Note 2**  If $K1$ AND $K2$ are not specified, they are calculated using the following equations:

$$K1 = \text{GAMMA2} - 2K2 \sqrt{\Phi_i - VBM}$$

$$K2 = \frac{(\text{GAMMA1} - \text{GAMMA2})(\sqrt{\Phi_i - VBX} - \sqrt{\Phi_i})}{2 \sqrt{\frac{\Phi_i}{\Phi_i - VBM}} - \sqrt{\Phi_i} + VBM}$$

where:

$$\Phi_i = 2V_t \cdot \ln\left(\frac{NCH}{n_i}\right)$$

$$V_t = \frac{k \cdot T}{q}$$

$$n_i = 1.45 \cdot 10^{10} \left(\frac{T}{300.15}\right)^{1.5} \exp\left(21.5565981 - \frac{E_g(T)}{2V_t}\right)$$
Circuit Modeling

Note 3  If $NCH$ is not given and $GAMMA1$ is given, then:

$$NCH = \frac{GAMMA1^2 \cdot (Cox)^2}{2q \cdot \varepsilon_{si}}$$

If neither $GAMMA1$ nor $NCH$ is given, then $NCH$ has a default value of $1.7e23 \, 1/m^3$ and $GAMMA1$ is calculated from $NCH$:

$$GAMMA1 = \sqrt{\frac{2q \cdot \varepsilon_{si} \cdot NCH}{Cox}}$$

If $GAMMA2$ is not given, then:

$$GAMMA2 = \sqrt{\frac{2q \cdot \varepsilon_{si} \cdot NSUB}{Cox}}$$

Note 3  If $CGSO$ is not given and $DLC>0$, then:

$$CGSO = (DLC \cdot Cox) - CGSL$$

If the previously calculated $CGSO<0$, then:

$CGSO=0$

Else:

$CGSO=0.6 \cdot XJ \cdot Cox$

Note 4  If $CGDO$ is not given and $DLC>0$, then:

$$CGDO = (DLC \cdot Cox) - CGSL$$

If the previously calculated $CGDO<0$, then

$CGDO=0$

Else:

$CGDO=0.6 \cdot XJ \cdot Cox$
Circuit Modeling

**Bipolar transistor**

**General form**

```
Q\{name\} \{ collector node\} \{ base node\} \{ emitter node\}
+ \{ substrate node\} \{ model name\} \{ area value\}
```

**Examples**

```
Q1 14 2 13 PNPNM
Q13 15 3 0 1 NPNSTRONG 1.5
Q7 VC 5 12 [SUB] LATPMP
```

**Model form**

```
.MODEL \{ model name\} NPN [model parameters]
.MODEL \{ model name\} PNP [model parameters]
.MODEL \{ model name\} LPNP [model parameters]
```

**Arguments and options**

- **[substrate node]**
  - is optional, and if not specified, the default is the ground.

- **[area value]**
  - is the relative device area and has a default value of 1.

**Description**

The bipolar transistor is modeled as an intrinsic transistor using ohmic resistances in series with the collector (RC/area), with the base (value varies with current, see Bipolar transistor equation), and with the emitter (RE/area).

![Diagram of Bipolar Transistor]

Positive current is current flowing into a terminal.
## MOSFET Model – **BSIM4 & BSIM5**

### BSIM4 Features

- Technology: < 100 nm, Tox < 30Å, High-k Material
- RF, Noise Model
- Pocket Implant, RSCE
- S/D R Model Enhancement
- Igate, Rg, Rsub, CTM, NQS, GIDL

### BSIM5 Features

- Technology: < 50 nm, Tox < 25Å, High-k Material
- RF, Noise Model, Quantum Mechanical Effect
- Pocket Implant, RSCE, Poly Gate Depletion
- S/D R Model Enhancement, Field Dependent Mobility
- Igate, Rg, Rsub, CTM, NQS, GIDL/GISL

### BSIM4 Application Target

- Sub 0.1 Tech. Application
- Accuracy, Efficiency, Scalability 향상
- Physical MP확보 및 Automated MPE System 개발

### BSIM5 Application Target

- Sub 50 nm Tech. Application
- Accuracy, Efficiency, Scalability 향상
- Physical MP확보 및 Automated MPE System 개발
Building on a strong foundation: BSIM4

Technology
- Short/Narrow Channel Effects on Threshold Voltage
- Non-Uniform Vertical and Lateral Doping Effects
- Mobility Reduction Due to Vertical Field
- Quantum Mechanic Effective Gate Oxide Thickness Model

Saturation
- Carrier Velocity Saturation
- Channel Length Modulation (CLM)
- Substrate Current Induced Body Effect (SCBE)
- Unified current saturation model (velocity saturation, velocity overshoot, source end velocity limit)

Leakage
- Gate Dielectric Tunneling Current Model
- Gate Induced Drain Current Model (GIDL)
- Trap assisted tunneling and recombination current model

RF
- RF Model (Gate & substrate resistance model)
- Unified Flicker Noise Model
- Holistic Thermal Noise Model

Parasitic
- Asymmetric Layout-dependent Parasitic Model
- Scalable stress effect model
Circuit Modeling

Effects Captured by BSIM5

- Gate tunneling model
- Stress effect model
- Impact Ionization model
- Flicker noise model
- Thermal noise model
- Saturation Model:
  - Velocity saturation
  - Velocity overshoot
  - Source end velocity limit
  - Channel length modulation;
  - Pocket doping effect
  - DIBL
  - Substrate current induced body effect
- Quantum mechanical effect
- Poly gate depletion
- Non-uniform doping model
- Short channel effect
- Narrow-width effect
- DIBL
- Bulk-charge effect
- Field-dependent mobility
- Non-Quasi-Static effect
- Diode IV and CV model
- Gate resistance model
- Substrate resistance network
- GIDL/GISL
- Asymmetric and bias-dependent source/drain resistance
Circuit Modeling

모델링 추세

- Deep SubMicron (DSM) Modeling
  - Design trend: Analog mixed simulation
  - Low voltage operation: Transition 부문에서의 smoothing 중 요
  - Process variation 예측: PCA 방법과 single set parameter
  - Non-Quasi-static modeling

- Parameter extraction의 중요성 증가

- High-Speed and RF modeling

- Public & Documentation for upgrade and world-wide usage

- Specific device modeling에 대한 필요성 증가
  - SOI model, TFT model, HVMOS(high voltage MOS) model 등
Circuit Modeling

DSM 모델인 BSIM3 특징

- Single I-V & Charge Equation
  - Model의 연속성이 향상되어 수렴특성에 타 모델에 비해 우수 (Scalability)
- Intrinsic, Extrinsic cap. 및 Narrow, Temperature, Output modeling 우수
  - Single Parameter set : global geometry region 표현 가능
  - Analog 회로 시뮬레이션에 대한 정확도 향상
- Public model / 표준 모델로 적용됨
  - Simulator간 Model Interface 문제 (Mixed Sim./CMI)를 해결
- Statistical Modeling에 적합
  - Design Centering에 필요한 모델 파라미터 추출 시 적합 (Physical, Single)
- 모델링 복잡성으로 Evaluation time은 증가하나 총 iteration은 감소함
  - Loading time이 증가됨 (1.5 ~ 2 배)
Circuit Modeling

Model Parameter Extraction

- In a truly “physics-based” model
  - Equations = General physics
  - Parameters = Specific situation
- In the real model (BSIM3, EKV etc.)
  - Equations = Empirical and physical
  - Parameters = must be extracted
- Model Quality
  - Heavily dependent on the parameter set quality (Extraction quality)

- Model parameter extraction
  - Model parameter extraction tool: BSIMpro, UMOST, APEX
  - Model parameter verification tool: MVP
RF modeling Issue

- Advantage of DSM MOSFET on Si at RF application
  - System-On-Chip
  - High density capability
  - Low cost
  - High $f_t$ (cut-off frequency)
  - Disadvantage - Substrate high freq. Coupling

- Design and optimize circuit operating in RF -> Exact RF model

- RF MOSFET modeling Issue
  - Accurate RF model
  - Reliable and Physics-based parameter extraction 기술 개발

- RF MOSFET modeling solution
  - Development of the Compact RF MOSFET model
  - MOSFET model (suitable to analog application) + Sub-circuit
  - RF 모델이 내장된 BSIM4 사용.
Physical Origin for RF MOSFET Modeling

- **Substrate resistance**
  - In low frequency
    - The impedance of junction capacitance de-couples the body potential from the drain voltage.
  - In RF
    - The impedance of junction capacitance is reduced → The voltage drop at substrate resistance increases.

\[ < \text{Schematic diagram for MOSFET} > \]
Physical Origin for RF MOSFET Modeling

- Gate resistance
  - In low frequency
    ✓ Rg ~ 0 (charging time << Time constant)
  - In RF
    ✓ NQS (non-quasi static, Rgch) + extra gate resistance (Reltd)

Diagram:

- NQS ~ Relmore (In BSIM3 V3.2)
- <Gate resistance>
Circuit Modeling

TFT (Thin Film Transistor) 모델링

- S-TFT(Samsung-TFT) model
  - Poly-Si TFT-LCD 회로 설계를 위한 물리적인 모델
  - 기존 모델 (RPI모델) 보다 정확도 및 성능이 우수함
    - Convergence 특성 우수 : 50% 이상
    - Simulation efficiency : 40% 이상 향상

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<th>Simplicity</th>
<th>RPI model</th>
<th>S-TFT model</th>
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<tbody>
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<td>복잡</td>
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<td>낮은 Vds에서 부정확</td>
<td>전 영역에서 정확</td>
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<td>Easy (PET)</td>
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</tr>
<tr>
<td>특징</td>
<td>Short channel 特성 모델링</td>
<td>물리적 모델</td>
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</tbody>
</table>

Ref : Presented in CICC2000
Circuit Modeling

S-TFT 모델의 적용 결과

- Large resistance
- Leakeage current
Circuit Modeling

SOI (Silicon-On-Insulator) 모델링

- **SOI Benefits**
  - **Performance**: 25~35% improvement (2Yrs. progress in bulk)
    - ✔ Junction capacitance 제거, Bulk effect (lower current: source not ground)
  - **Low Power**: 2X improvement

![Graph showing performance and power consumption over time.](image)

Above are actual figures derived in lab tests using SOI-based chips

Ref: [IBM]
Circuit Modeling

SOI (Silicon-On-Insulator) 모델링

- Honeywell model
- BTASOI model
- UFSOI model
  - Short channel effect모델 빈약
  - PD/FD/DD model
- BSIM3SOI model
  - BSIM3 v3.1 모델을 기본으로 함
  - Public model
  - PD/FD/DD model
HVMOS (High voltage MOS) 모델링

- HVMOS device의 용도
  - LCD Driver Ic (LDI) : 20 ~ 30V range
  - Flash driver : 15~20V range
    - (PDP driver IC : 200V 이상)

- HVMOS 소자의 특징
  - External Rds의 비대칭과 bias 의존성
  - Mobility degradation의 Vds 의존성
  - High Vgs에서 gm의 감소 (saturation)
  - SCBE Gate-voltage Dependence
  - A0의 temperature dependence
  - Vsat의 bias dependence
  - Self-heating Effect

일반 MOS 모델 적용 불가능
일반 MOS vs. HVMOS model parameter 추출 결과

- HVMOS 모델의 I-V 데이터 및 회로 측정치 대비 정확도 우수

Vgs에 따른 전류특성 오차 심함

BSIM3 모델 파라미터 추출 결과

HVMOS 모델 파라미터 추출 결과
**SEC. 3.9 – MODELS FOR SIMULATION OF MOS CIRCUITS**

**FET Model Generations**

- First Generation – Physically based analytical model including all geometry dependence.
- Second Generation – Model equations became subject to mathematical conditioning for circuit simulation. Use of empirical relationships and parameter extraction.
- Third Generation – A return to simpler model structure with reduced number of parameters which are physically based rather than empirical. Uses better methods of mathematical conditioning for simulation including more specialized smoothing functions.

**Performance Comparison of Models** (from Cheng and Hu, *MOSFET Modeling & BSIM3 Users Guide*):

<table>
<thead>
<tr>
<th>Model</th>
<th>Minimum L (μm)</th>
<th>Minimum Tox (nm)</th>
<th>Model Continuity</th>
<th>$i_D$ Accuracy in Strong Inversion</th>
<th>$i_D$ Accuracy in Subthreshold</th>
<th>Small signal parameter</th>
<th>Scalability</th>
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<tbody>
<tr>
<td>MOS1</td>
<td>5</td>
<td>50</td>
<td>Poor</td>
<td>Poor</td>
<td>Not Modeled</td>
<td>Poor</td>
<td>Poor</td>
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<tr>
<td>MOS2</td>
<td>2</td>
<td>25</td>
<td>Poor</td>
<td>Poor</td>
<td>Poor</td>
<td>Poor</td>
<td>Fair</td>
</tr>
<tr>
<td>MOS3</td>
<td>1</td>
<td>20</td>
<td>Poor</td>
<td>Fair</td>
<td>Poor</td>
<td>Poor</td>
<td>Poor</td>
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<tr>
<td>BSIM1</td>
<td>0.8</td>
<td>15</td>
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<td>Good</td>
<td>Fair</td>
<td>Poor</td>
<td>Fair</td>
</tr>
<tr>
<td>BSIM2</td>
<td>0.35</td>
<td>7.5</td>
<td>Fair</td>
<td>Good</td>
<td>Good</td>
<td>Fair</td>
<td>Fair</td>
</tr>
<tr>
<td>BSIM3v2</td>
<td>0.25</td>
<td>5</td>
<td>Fair</td>
<td>Good</td>
<td>Good</td>
<td>Good</td>
<td>Good</td>
</tr>
<tr>
<td>BSIM3v3</td>
<td>0.15</td>
<td>4</td>
<td>Good</td>
<td>Good</td>
<td>Good</td>
<td>Good</td>
<td>Good</td>
</tr>
</tbody>
</table>
First Generation Models

Level 1 (MOS1)
- Basic square law model based on the gradual channel approximation and the square law for saturated drain current.
- Good for hand analysis.
- Needs improvement for deep-submicron technology (must incorporate the square law to linear shift)

Level 2 (MOS2)
- First attempt to include small geometry effects
- Inclusion of the channel-bulk depletion charge results in the familiar 3/2 power terms
- Introduced a simple subthreshold model which was not continuous with the strong inversion model.
- Model became quite complicated and probably is best known as a “developing ground” for better modeling techniques.

Level 3 (MOS3)
- Used to overcome the limitations of Level 2. Made use of a semi-empirical approach.
- Added DIBL and the reduction of mobility by the lateral field.
- Similar to Level 2 but considerably more efficient.
- Used binning but was poorly implemented.
Second Generation Models
BSIM (Berkeley Short-Channel IGFET Model)
- Emphasis is on mathematical conditioning for circuit simulation
- Short channel models are mostly empirical and shifts the modeling to the parameter extraction capability
- Introduced a more detailed subthreshold current model with good continuity
- Poor modeling of channel conductance

HSPICE Level 28
- Based on BSIM but has been extensively modified.
- More suitable for analog circuit design
- Uses model binning
- Model parameter set is almost entirely empirical
- User is locked into HSPICE
- Model is proprietary

BSIM2
- Closely based on BSIM
- Employs several expressions developed from two dimensional analysis
- Makes extensive modifications to the BSIM model for mobility and the drain current
- Uses a new subthreshold model
- Output conductance model makes the model very suitable for analog circuit design
- The drain current model is more accurate and provides better convergence
- Becomes more complex with a large number of parameters
- No provisions for variations in the operating temperature
Circuit Modeling

Third Generation Models

BSIM3
- This model has achieved stability and is being widely used in industry for deep submicron technology.
- Initial focus of simplicity was not realized.

MOS Model 9
- Developed at Philips Laboratory
- Has extensive heritage of industrial use
- Model equations are clean and simple – should be efficient

Other Candidates
- EKV (Enz-Krummenacher-Vittoz) – fresh approach well suited to the needs of analog circuit design
Circuit Modeling

BSIM2 Model
Generic composite expression for the model parameters:

\[ X = X_0 + \frac{LX}{L_{\text{eff}}} + \frac{WX}{W_{\text{eff}}} \]

where

- \( X_0 \) = parameter for a given \( W \) and \( L \)
- \( LX \) (\( WX \)) = first-order dependence of \( X \) on \( L \) (\( W \))

Modeling features of BSIM2:

Mobility
- Mobility reduction by the vertical field
- Mobility reduction by the lateral field

Drain Current
- Velocity saturation
- Linear region drain current
- Saturation region drain current
- Subthreshold current

\[ i_{DS} = \mu_0 C_{Ox} W_{\text{eff}} \frac{(kT)^2}{q} \frac{e^{v_{GS}-v_{T}-V_{\text{off}}}}{n} \cdot [1 - e^{qV_{DS}/kT}] \]

where

\[ V_{\text{off}} = V_{OF} + V_{OFB} \cdot v_{BS} + V_{OFD} \cdot v_{DS} \quad \text{and} \quad n = NO + \frac{NB}{\sqrt{PHI - v_{BS}}} + ND \cdot v_{DS} \]
Circuit Modeling

**BSIM2 Output Conductance Model**

- Drain-Induced Barrier Lowering (DIBL) – Lowering of the potential barrier at the source-bulk junction allowing carriers to traverse the channel at a lower gate bias than would otherwise be expected.

- Substrate Current-Induced Body Effect (SCBE) – The high field near the drain accelerates carriers to high energies resulting in impact ionization which generates a hole-electron pair (hot carrier generation). The opposite carriers are swept into the substrate and have the effect of slightly forward-biasing the source-substrate junction. This reduces the threshold voltage and increases the drain current.

**Charge Model**
- Eliminates the partitioning choice (50%/50% is used)
- BSIM charge model better documented with more options
BSIM2 Basic Parameter Extraction

- A number of devices with different W/L are fabricated and measured.

- A long, wide device is used as the base to add geometry effects as corrections.
- Procedure:
  1.) Oxide thickness and the differences between the drawn and effective channel dimensions are provided as process input.
  2.) A long, wide device is used to determine some base parameters which are used as the starting point for each individual device extraction in the second phase.
  3.) In the second phase, a set of parameters is extracted independently for each device. This phase represents the fitting of the data for each independent device to the intrinsic equation structure of the model.
  1.) In the third phase, the compiled parameters from the second phase are used to determine the geometry parameters. This represents the imposition of the extrinsic structure onto the model.
Circuit Modeling

BSIM2 Model used in Subthreshold
BSIM Model Parameters used in Subthreshold
VDS 1.0 DC 3.0
M1 1 I 0 0 CMOSN W=5UM L=2UM
.MODEL CMOSN NMOS LEVEL=4
+VFB=-7.92628E-01 LVB= 1.22972E-02 WVF= -1.00233E-01
+PHI= 7.59099E-01 LPHI= 0.00000E+00 WPHI= 0.00000E+00
+K1= 1.06705E+00 LK1= 5.08430E-02 WK= 4.72787E-01
+K2= -4.23365E-03 LK2= 6.76974E-02 WK= 6.27415E-02
+ETA= -4.30579E-03 LETA= 9.05179E-03 WETA= 7.33154E-03
+MIZ= 5.58459E+02 DL= 6.86137E-001 DW= -1.04701E-001
+U0= 5.52698E-02 LU0= 6.09430E-02 WU0= -6.91423E-02
+U1= 5.38133E-03 LU1= 5.43387E-01 WU1= -8.63357E-02
+X2M= 1.45214E+01 LX2M= -3.08694E+01 WX2M= 4.75033E+01
+X2E= -1.67104E-04 LX2E= -4.75323E-03 WX2E= -2.74841E-03
+X3E= 5.33407E-04 LX3E= -4.69455E-04 WX3E= -5.26199E-03
+X2U= 2.45645E-03 LX2U= -1.46188E-02 WX2U= -2.35555E-02
+X2U= 3.80979E-04 LX2U= -1.71488E-03 WX2U= -2.35200E-02
+MUS= 5.48735E+02 LMUS= 3.28720E+02 WMUS= 1.35360E+02
+X2M= 6.72261E+00 LX2M= -3.48094E+01 WX2M= 9.84809E+01
+X3M= -2.79427E+00 LX3M= 6.31555E+01 WX3M= -1.99720E-01
+X3U= 1.18671E-03 LX3U= 6.13936E-02 WX3U= -3.49351E-03
+TOX= 4.30000E-02 TEM= 2.70000E+00 VDD= 5.00000E+00
+CGDO= 4.40942E-01 CGSO= 4.40942E-01 CGBO= 6.34142E-01
+XPART= 1.00000E+000
+N0= 1.00000E+000 LNO= 0.00000E+000 WNO= 0.00000E+000
+N= 0.00000E+000 LNB= 0.00000E+000 WNB= 0.00000E+000
+N= 0.00000E+000 LND= 0.00000E+000 WND= 0.00000E+000
+RSH= 0 CJ= 4.141500e-04 CJSW= 4.617400e-10 JS= 0 PB= 0.8
+PBSW= 0.8 MJ= 0.4726 MJSW= 0.3597 WDF= 0 DELL= 0
.DC VDS 5.0 0 0 0.01
.PRINT DC ID(M1)
.PROBE
.END

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Circuit Modeling

Results of the BSIM2 Model Simulation in Subthreshold

Graph showing the relationship between drain current (ID) and gate-source voltage (VGS) for a MOSFET in subthreshold region.
BSIM3 Model
The short channel effects included in the BSIM3 model are:
• Normal and reverse short-channel and narrow-width effects on the threshold.
• Channel length modulation (*CLM*).
• Drain induced barrier lowering (*DIBL*).
• Velocity saturation.
• Mobility degradation due to the vertical electric field.
• Impact ionization.
• Band-to-band tunnelling.
• Velocity overshoot.
• Self-heating.
1. Channel quantiztion.
2. Polysilicon depletion.
BSIM3v3 Model Equations for Hand Calculations

In strong inversion, approximate hand equations are:

\[ i_{DS} = \mu_{eff} C_{ox} \frac{W_{eff}}{L_{eff}} \frac{1}{1 + \frac{E_{sat}}{E_{sat} L_{eff}}} \left( v_{GS} - v_{th} - A_{bulk} V_{DS} \right) \left( v_{DS} - \frac{V_{DS}(sat)}{2} \right) \], \quad v_{DS} < V_{DS}(sat)

\[ i_{DS} = W_{eff} v_{sat} C_{ox} [v_{GS} - v_{th} - A_{bulk} V_{DS}(sat)] \left( 1 + \frac{v_{DS} - V_{DS}(sat)}{V_{A}} \right), \quad v_{DS} > V_{DS}(sat) \]

where

\[ V_{DS}(sat) = \frac{E_{sat} L_{eff} (v_{GS} - v_{th})}{A_{bulk} E_{sat} L_{eff} + (v_{GS} - v_{th})} \]

\[ L_{eff} = L_{drawn} - 2dL \]

\[ W_{eff} = W_{drawn} - 2dW \]

\[ E_{sat} = \text{Electric field where the drift velocity (v) saturates} \]

\[ v_{sat} = \text{saturation velocity of carriers in the channel} \]

\[ \mu = \frac{\mu_{eff}}{1 + (E_{y}/E_{sat})} \Rightarrow \mu_{eff} = \frac{2v_{sat}}{E_{sat}} \]

Note: Assume \( A_{bulk} \approx 1 \) and extract \( V_{th} \) and \( V_{A} \).
Circuit Modeling

MOSIS Parametric Test Results

http://www.mosis.org/

RUN: T02D  
TECHNOLOGY: SCN025  
VENDOR: TSMC  
FEATURE SIZE: 0.25 microns

INTRODUCTION: This report contains the lot average results obtained by MOSIS from measurements of MOSIS test structures on each wafer of this fabrication lot. SPICE parameters obtained from similar measurements on a selected wafer are also attached.

COMMENTS: TSMC 0251P5M.

<table>
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<tr>
<th>TRANSISTOR PARAMETERS</th>
<th>W/L</th>
<th>N-CHANNEL</th>
<th>P-CHANNEL</th>
<th>UNITS</th>
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<td>uA/um</td>
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<td>Gamma</td>
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<td>0.61</td>
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<td>112.0</td>
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<td>uA/V2</td>
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</table>

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0.25μm BSIM3v3.1 NMOS Parameters

.CMODEL CMOSN NMOS ( LEVEL = 49
+VERSION = 3.1  TNOM = 27  TOX = 5.7E-9
+XJ = 1E-7  NCH = 2.3549E17  VTH0 = 0.4273342
+K1 = 0.3922983  K2 = 0.0185825  K3 = 1E-3
+K3B = 2.0947677  W0 = 2.171779E-7  NLX = 1.919758E-7
+DVT0W = 0  DVT1W = 0  DVT2W = 0
+DVT0 = 7.137212E-3  DVT1 = 6.066487E-3  DVT2 = -0.3025397
+U0 = 403.1776038  UA = -3.60743E-12  UB = 1.323051E-18
+UC = 2.575123E-11  VSAT = 1.616298E5  A0 = 1.4626549
+AGS = 0.3136349  B0 = 3.080869E-8  B1 = -1E-7
+KETA = 5.462411E-3  A1 = 4.653219E-4  A2 = 0.6191129
+RDSW = 345.624986  PRWG = 0.3183394  PRWB = -0.1441065
+WR = 1  WINT = 8.107812E-9  LIN = 3.375523E-9
+XL = 3E-8  XW = 0  DWG = 6.420502E-10
+DWB = 1.042094E-8  VOFF = -0.1083577  NFACTOR = 1.1884386
+CT = 0  CDSC = 2.4E-4  CDSCD = 0
+CDSCB = 0  ETA0 = 4.914545E-3  ETAB = 4.215338E-4
+DSUB = 0.0313287  PCLM = 1.2088426  PDIBLC1 = 0.7240447
+PDIBLC2 = 5.120303E-3  PDIBLCB = -0.0443076  DROUT = 0.7752992
+PSCBE1 = 4.451333E8  PSCBE2 = 5E-10  PVAG = 0.2068286
+DELTA = 0.01  MOBMOD = 1  PRT = 0
+UTE = -1.5  KT1 = -0.11  KTIL = 0
+KT2 = 0.022  UA1 = 4.31E-9  UB1 = -7.61E-18
+UC1 = -5.6E-11  AT = 3.3E4  WL = 0
+WLW = 1  WW = -1.22182E-16  WWN = 1.2127
+WWL = 0  LL = 0  LLN = 1
+LW = 0  LWN = 1  LWL = 0
+CAPMOD = 2  XPAR = 0.4  CGDO = 6.33E-10
+CGSO = 6.33E-10  CGBO = 1E-11  CJ = 1.766171E-3
+PB = 0.9577677  MJ = 0.4579102  CJSW = 3.931544E-10
+PBSW = 0.99  MJSW = 0.2722644  CF = 0
+PVTH0 = -2.126483E-3  PRDSW = -24.2435379  PK2 = -4.788094E-4
+WKETA = 1.430792E-3  LKETA = -6.548592E-3
)

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Circuit Modeling

0.25μm BSIM3v3.1 PMOS Parameters

MODEL CMOS PMOS ( LEVEL = 49
+VERSION = 3.1 TNOM = 27 TOX = 5.7E-9
+XJ = 1E-7 NCH = 4.1589E17 VTH0 = -0.6193382
+K1 = 0.5275326 K2 = 0.0281819 K3 = 0
+K3B = 11.249555 W0 = 1E-6 NLX = 1E-9
+DVT0W = 0 DVT1W = 0 DVT2W = 0
+DVT0 = 3.1920483 DVT1 = 0.4901788 DVT2 = -0.0295257
+U0 = 185.1288894 UA = 3.40616E-9 UB = 3.640498E-20
+UC = -6.35238E-11 VSAT = 1.975064E5 A0 = 0.4156696
+AGS = 0.0702036 B0 = 3.111154E-6 B1 = 5E-6
+KETA = 0.0253118 A1 = 2.421043E-4 A2 = 0.6754231
+RDSW = 866.896668 PRWG = 0.0362726 PRWB = -0.293946
+WR = 1 WINT = 6.519911E-9 LINT = 2.210804E-8
+XL = 3E-8 XW = 0 DWG = -2.423118E-8
+DWB = 3.052612E-8 VOFF = -0.1161062 NFACTOR = 1.2546896
+CIT = 0 CDSC = 2.4E-4 CDSCD = 0
+CDSCB = 0 ETA0 = 0.7241245 ETAB = -0.3675267
+DSUB = 1.1734643 PCLM = 1.0837457 PDIBLC1 = 9.608442E-4
+PDIBLC2 = 0.0176785 PDIBLCB = -9.605935E-4 DROUT = 0.0735541
+PSCBE1 = 1.579442E10 PSCBE2 = 6.707105E-9 PVAG = 0.0409261
+DELTAB = 0.01 MOBMOD = 1 PRT = 0
+UTE = -1.5 KT1 = -0.11 KT1L = 0
+KT2 = 0.022 UA1 = 4.31E-9 UB1 = -7.61E-18
+UC1 = -5.6E-11 AT = 3.3E4 WL = 0
+WLN = 1 WW = 0 WWN = 1
+WWL = 0 LL = 0 LLN = 1
+LW = 0 LWN = 1 LWL = 0
+CAPMOD = 2 XPART = 0.4 CGDO = 5.11E-10
+CGSO = 5.11E-10 CGBO = 1E-11 CJ = 1.882953E-3
+PB = 0.99 MJ = 0.4690946 CJSW = 3.018356E-10
+PBSW = 0.8137064 MJSW = 0.3299497 CF = 0
+PVTH0 = 5.268963E-3 PRDSW = -2.2622317 PK2 = 3.952008E-3
+WKE = -7.69819E-3 LKE = -0.0119828 )

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Circuit Modeling

Adjustable Precision Analog Models – Table Lookup

- Objective
  Develop models having adjustable precision in ac and dc performance using table lookup models.

- Advantages
  Usable at any level – device, circuit, or behavioral
  Quickly developed from experiment or process simulators
  Faster than analytical device models (BSIM)

- Disadvantages
  Requires approximately 10kbytes for a typical MOS model
  Can’t be parameterized easily
Summary of MOSFET Models for Simulation

- Models are much improved for efficient computer simulation
- Output conductance model is greatly improved
- Poor results for narrow channel transistors
- Can have discontinuities at bin boundaries
- Fairly complex model, difficult to understand in detail
SEC. 3.10 – EXTRACTION OF A LARGE SIGNAL MODEL FOR HAND CALCULATIONS

Objective

Extract a simple model that is useful for design from the computer models such as BSIM3.

Extraction for Short Channel Models

Procedure for extracting short channel models:

1.) Extract the square-law model parameters for a transistor with length at least 10 times $L_{\text{min}}$.

2.) Using the values of $K'$, $V_T$, $\lambda$, and $\gamma$ extract the model parameters for the following model:

$$i_D = \frac{K'}{2[1 + \theta(v_{GS} - V_T)]} \frac{W}{L} \left[ v_{GS} - V_T \right]^2 (1 + \lambda v_{DS})$$

Adjust the values of $K'$, $V_T$, and $\lambda$ as needed.
EXTRACTION OF THE SIMPLE, SQUARE-LAW MODEL

Characterization of the Simple Square-Law Model

Equations for the MOSFET in strong inversion:

\[ i_D = K \left( \frac{W_{\text{eff}}}{2L_{\text{eff}}} \right) (v_{GS} - V_T) \frac{1}{2} (1 + \lambda v_{DS}) \]  \hspace{1cm} (1)

\[ i_D = K \left( \frac{W_{\text{eff}}}{L_{\text{eff}}} \right) \left[ (v_{GS} - V_T)v_{DS} - \frac{v_{DS}^2}{2} \right] (1 + \lambda v_{DS}) \]  \hspace{1cm} (2)

where

\[ V_T = V_{T0} + \gamma \left[ \sqrt{2|\phi_F|} + v_{SB} - \sqrt{2|\phi_F|} \right] \]  \hspace{1cm} (3)
Extraction of Model Parameters:

First assume that \( v_{DS} \) is chosen such that the \( \lambda v_{DS} \) term in Eq. (2) is much less than one and \( v_{SB} \) is zero, so that \( V_T = V_{T0} \).

Therefore, Eq. (2) simplifies to

\[
i_D = K' \left( \frac{W_{\text{eff}}}{2L_{\text{eff}}} \right) (v_{GS} - V_{T0})^2
\]

(6)

This equation can be manipulated algebraically to obtain the following

\[
i_D^{1/2} = \left( \frac{K' W_{\text{eff}}}{2L_{\text{eff}}} \right)^{1/2} v_{GS} = \left( \frac{K' W_{\text{eff}}}{2L_{\text{eff}}} \right)^{1/2} V_{T0}
\]

(7)

which has the form

\[
y = mx + b
\]

(8)

This equation is easily recognized as the equation for a straight line with \( m \) as the slope and \( b \) as the \( y \)-intercept. Comparing Eq. (7) to Eq. (8) gives

\[
y = i_D^{1/2}
\]

(9)

\[
x = v_{GS}
\]

(10)

\[
m = \left( \frac{K' W_{\text{eff}}}{2L_{\text{eff}}} \right)^{1/2}
\]

(11)

and

\[
b = -\left( \frac{K' W_{\text{eff}}}{2L_{\text{eff}}} \right)^{1/2} V_{T0}
\]

(12)
Illustration of $K'$ and $V_T$ Extraction

\[ (i_D)^{1/2} \]

\[ V_{DS} > V_{DSAT} \]

Weak inversion region

\[ \mu = \left( \frac{K' W_{eff}}{2L_{eff}} \right)^{1/2} \]

Mobility degradation region

Comments:
- Stay away from the extreme regions of mobility degradation and weak inversion
- Use channel lengths greater than $L_{min}$
Transfer Characteristics : Output Characteristics (Linear Region)

Output Drain current as a function of the input gate bias for fixed drain bias:

\[ I_D = \frac{Z}{L} \bar{V}_d C_i [V_G - V_T] V_D \]

Figure 6—28
Linear region transfer characteristics: (a) plot of drain current versus gate voltage for MOSFETs in the linear region; (b) transconductance as a function of gate bias.
Transfer Characteristics: Output Characteristics (Saturation Region)

- Square root of Drain current as a function of the input gate bias:

\[ \sqrt{I_{D\text{sat}}} = \sqrt{\frac{k_N\text{(sat)}}{2}} (V_G - V_T) \]

Figure 6—29
Saturation region transfer characteristics: plot of square root of the drain current versus gate voltage for MOSFETs.
Example 3.10-1 – Extraction of $K'$ and $V_T$ Using Linear Regression

Given the following transistor data shown in Table 3.10-1 and linear regression formulas based on the form,

$$y = mx + b$$

and

$$m = \frac{\sum x_i y_i - (\sum x_i \sum y_i)/n}{\sum x_i^2 - (\sum x_i)^2/n}$$

(13)

(14)

determine $V_{T0}$ and $K W/2L$. The data in Table B-1 also give $I_D^{1/2}$ as a function of $V_{GS}$.

Table 3.10-1 Data for Example 3.10-1

<table>
<thead>
<tr>
<th>$V_{GS}$ (V)</th>
<th>$I_D$ (μA)</th>
<th>$\sqrt{I_D}$ (μA)$^{1/2}$</th>
<th>$V_{SB}$ (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.000</td>
<td>0.700</td>
<td>0.837</td>
<td>0.000</td>
</tr>
<tr>
<td>1.200</td>
<td>2.00</td>
<td>1.414</td>
<td>0.000</td>
</tr>
<tr>
<td>1.500</td>
<td>8.00</td>
<td>2.828</td>
<td>0.000</td>
</tr>
<tr>
<td>1.700</td>
<td>13.95</td>
<td>3.735</td>
<td>0.000</td>
</tr>
<tr>
<td>1.900</td>
<td>22.1</td>
<td>4.701</td>
<td>0.000</td>
</tr>
</tbody>
</table>
Example 3.10-1 – Continued

Solution

The data must be checked for linearity before linear regression is applied. Checking slopes between data points is a simple numerical technique for determining linearity. Using the formula that

\[
\text{Slope} = m = \frac{\Delta y}{\Delta x} = \frac{\sqrt{I_{D2}} - \sqrt{I_{D1}}}{V_{GS2} - V_{GS1}}
\]

Gives

\[
m_1 = \frac{1.414 - 0.837}{0.2} = 2.885 \\
m_2 = \frac{2.828 - 1.414}{0.3} = 4.713 \\
m_3 = \frac{3.735 - 2.828}{0.2} = 4.535 \\
m_4 = \frac{4.701 - 3.735}{0.2} = 4.830
\]

These results indicate that the first (lowest value of \( V_{GS} \)) data point is either bad, or at a point where the transistor is in weak inversion. This data point will not be included in subsequent analysis. Performing the linear regression yields the following results.

\[
V_{T0} = 0.898 \text{ V} \quad \text{and} \quad \frac{K'W_{\text{eff}}}{2L_{\text{eff}}} = 21.92 \mu A/V^2
\]
Extraction of the Bulk-Threshold Parameter $\gamma$

Using the same techniques as before, the following equation

$$V_T = V_{T0} + \gamma [\sqrt{2|\phi_F|} + v_{SB} - \sqrt{2|\phi_F|}]$$

is written in the linear form where

$$y = V_T$$

$$x = \sqrt{2|\phi_F|} + v_{SB} - \sqrt{2|\phi_F|}$$

$$m = \gamma$$

$$b = V_{T0}$$

The term $2|\phi_F|$ is unknown but is normally in the range of 0.6 to 0.7 volts.

Procedure:

1.) Pick a value for $2|\phi_F|$.
2.) Extract a value for $\gamma$.
3.) Calculate $N_{SUB}$ using the relationship,

$$\gamma = \frac{\sqrt{2} \varepsilon_{si} q N_{SUB}}{C_{ox}}$$

4.) Calculate $\phi_F$ using the relationship,

$$\phi_F = -\frac{kT}{q} \ln \left( \frac{N_{SUB}}{n_i} \right)$$

5.) Iterative procedures can be used to achieve the desired accuracy of $\gamma$ and $2|\phi_F|$. Generally, an approximate value for $2|\phi_F|$ gives adequate results.
Illustration of the Procedure for Extracting $\gamma$

A plot of $\sqrt{i_D}$ versus $v_{GS}$ for different values of $v_{SB}$ used to determine $\gamma$ is shown below.

By plotting $V_T$ versus $x$ of Eq. (19) one can measure the slope of the best fit line from which the parameter $\gamma$ can be extracted. In order to do this, $V_T$ must be determined at various values of $v_{SB}$ using the technique previously described.
Illustration of the Procedure for Extracting γ - Continued

Each $V_T$ determined above must be plotted against the $v_{SB}$ term. The result is shown below. The slope $m$, measured from the best fit line, is the parameter $γ$.

$$
(V_T \text{ vs. } v_{SB})
$$

$$
V_{SB} = 0V \quad V_{SB} = 1V \quad V_{SB} = 2V \quad V_{SB} = 3V
$$

$$
(m = γ)
$$

$$(v_{SB} + 2|\Phi_F|)^{0.5} - (2|\Phi_F|)^{0.5}$$

FigAppB-03
Example 3.10-2 – Extraction of the Bulk Threshold Parameter

Using the results from Ex. B-1 and the following transistor data, determine the value of $\gamma$ using linear regression techniques. Assume that $2|\phi_f|$ is 0.6 volts.

<table>
<thead>
<tr>
<th>$V_{SB}$ (V)</th>
<th>$V_{GS}$ (V)</th>
<th>$I_D$ (\mu A)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.000</td>
<td>1.400</td>
<td>1.431</td>
</tr>
<tr>
<td>1.000</td>
<td>1.600</td>
<td>4.55</td>
</tr>
<tr>
<td>1.000</td>
<td>1.800</td>
<td>9.44</td>
</tr>
<tr>
<td>1.000</td>
<td>2.000</td>
<td>15.95</td>
</tr>
<tr>
<td>2.000</td>
<td>1.700</td>
<td>3.15</td>
</tr>
<tr>
<td>2.000</td>
<td>1.900</td>
<td>7.43</td>
</tr>
<tr>
<td>2.000</td>
<td>2.10</td>
<td>13.41</td>
</tr>
<tr>
<td>2.000</td>
<td>2.30</td>
<td>21.2</td>
</tr>
</tbody>
</table>

**Solution**

Table B-2 shows data for $V_{SB} = 1$ volt and $V_{SB} = 2$ volts. A quick check of the data in this table reveals that $\sqrt{I_D}$ versus $V_{GS}$ is linear and thus may be used in the linear regression analysis. Using the same procedure as in Ex. B-1, the following thresholds are determined: $V_{T_0} = 0.898$ volts (from Ex. B-1), $V_T = 1.143$ volts (@ $V_{SB} = 1$ V), and $V_T = 1.322$ V (@ $V_{SB} = 2$ V). Table B-3 gives the value of $V_T$ as a function of $[(2|\phi_f| + V_{SB})^{1/2} - (2|\phi_f|)^{1/2}]$ for the three values of $V_{SB}$.
**Example 3.10-2 - Continued**

Table 3.10-3 Data for Example 3.10-2.

| $V_{SB}$ (V) | $V_T$ (V) | $[\sqrt{2|\phi_F| + V_{SB}} - \sqrt{2|\phi_F|}]$ (V$^{1/2}$) |
|--------------|-----------|---------------------------------------------------|
| 0.000        | 0.898     | 0.000                                             |
| 1.000        | 1.143     | 0.490                                             |
| 2.000        | 1.322     | 0.838                                             |

With these data, linear regression must be performed on the data of $V_T$ versus $[(2|\phi_F| + V_{SB})^{0.5} - (2|\phi_F|)^{0.5}]$. The regression parameters of Eq. (13) are

\[
\Sigma x_i y_i = 1.668
\]

\[
\Sigma x_i^2 y_i = 4.466
\]

\[
\Sigma x_i^2 = 0.9423
\]

\[
(\Sigma x_i)^2 = 1.764
\]

These values give $m = 0.506 = \gamma$.  

---

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Circuit Modeling

Extraction of the Channel Length Modulation Parameter, $\lambda$

The channel length modulation parameter $\lambda$ should be determined for all device lengths that might be used. For the sake of simplicity, Eq. (2) is rewritten as

$$i_D = i_D' - \lambda' v_{DS} + i_D'$$

which is in the familiar linear form where

$$y = i_D \text{ (Eq. (2))}$$
$$x = v_{DS}$$
$$m = \lambda i_D'$$
$$b = i_D' \text{ (Eq. (2) with } \lambda = 0)$$

By plotting $i_D$ versus $v_{DS}$, measuring the slope of the data in the saturation region, and dividing that value by the $y$-intercept, $\lambda$ can be determined. The procedure is illustrated in the figure shown.
Example 3.10-3 – Extraction of the Channel Length Modulation Parameter

Given the data of $I_D$ versus $V_{DS}$ in Table 10.3-4, determine the parameter $\lambda$.

<table>
<thead>
<tr>
<th>$I_D$ (μA)</th>
<th>39.2</th>
<th>68.2</th>
<th>86.8</th>
<th>94.2</th>
<th>95.7</th>
<th>97.2</th>
<th>98.8</th>
<th>100.3</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{DS}$ (V)</td>
<td>0.500</td>
<td>1.000</td>
<td>1.500</td>
<td>2.000</td>
<td>2.50</td>
<td>3.00</td>
<td>3.50</td>
<td>4.00</td>
</tr>
</tbody>
</table>

**Solution**

We note that the data of Table 3.10-4 covers both the saturation and nonsaturation regions of operation. A quick check shows that saturation is reached near $V_{DS} = 2.0$ V. To calculate $\lambda$, we shall use the data for $V_{DS}$ greater than or equal to 2.5 V. The parameters of the linear regression are

$$x_i y_i = 1277.85$$

$$\sum x_i \sum y_i = 5096.00$$

$$\sum x_i^2 = 43.5$$

$$(\sum x_i)^2 = 169$$

These values result in $m = \lambda I'_D = 3.08$ and $b = I'_D = 88$, giving $\lambda = 0.035$ V$^{-1}$.

The slope in the saturation region is typically very small, making it necessary to be careful that two data points taken with low resolution are not subtracted (to obtain the slope) resulting in a number that is of the same order of magnitude as the resolution of the data point measured. If this occurs, then the value obtained will have significant and unacceptable error.
Circuit Modeling

EXTRACTION OF THE SIMPLE MODEL FOR SHORT CHANNEL MOSFETS

Extraction for Short Channel MOSFETS

The model proposed is the following one which is the square-law model modified by the velocity saturation influence.

\[ i_D = \frac{K'}{2[1 + \theta(V_{GS}-V_T)]} \frac{W}{L} [v_{GS} - V_T]^2(1+\lambda v_{DS}) \]

Using the values of \( K' \), \( V_T \), \( \lambda \), and \( \gamma \) extracted previously, use an appropriate extraction procedure to find the value of \( \theta \) adjusting the values of \( K' \), \( V_T \), and \( \lambda \) as needed.

Comments:

- We will assume that the bulk will be connected to the source or the standard relationship between \( V_T \) and \( V_{BS} \) can be used.
- The saturation voltage is still given by

\[ V_{DS(\text{sat})} = V_{GS} - V_T \]
Example of a Genetic Algorithm

1.) To use this algorithm or any other, use the simulator and an appropriate short-channel model (BSIM3) to generate a set of data for the transconductance ($i_D$ vs. $v_{GS}$) and output characteristics ($i_D$ vs. $v_{DS}$) of the transistor with the desired $W$ and $L$ values.

2.) The best fit to the data is found using a genetic algorithm. The constraints on the parameters are obtained from experience with prior transistor parameters and are:

$$10 \text{E}-6 < \beta < 6 \text{E}-6, \quad 1 < \theta < 5, \quad 0 < V_T < 1, \quad \text{and} \quad 0 < \lambda < 0.5$$

3.) The details of the genetic algorithm are:

Gene structure is $A = [\beta, \theta, V_T, \text{fitness}]$. A mutation was done by varying all four parameters. A weighted sum of the least square errors of the data curves was used as the error function. The fitness of a gene was chosen as $1/\text{error}$.

4.) The results for an extraction run of 8000 iterations for an NMOS transistor is shown below.

<table>
<thead>
<tr>
<th>$\beta$(A/V$^2$)</th>
<th>$\theta$</th>
<th>$V_T$(V)</th>
<th>$\lambda$(V$^{-1}$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>294.1x10$^{-6}$</td>
<td>1.4564</td>
<td>0.4190</td>
<td>0.1437</td>
</tr>
</tbody>
</table>

5.) The results for a NMOS and PMOS transistor are shown on the following pages.

---


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Extraction Results for an NMOS Transistor with $W = 0.32\mu m$ and $L = 0.18\mu m$

Transconductance:

![Graph showing IDS vs. VGS for an NMOS transistor with $W = 0.32\mu m$ and $L = 0.18\mu m$. The graph includes measured data and a curve fit.](image-url)
Extraction Results for an NMOS Transistor with $W = 0.32\mu m$ and $L = 0.18\mu m$

Output:
Extraction Results for an PMOS Transistor with $W = 0.32\mu m$ and $L = 0.18\mu m$

Transconductance:
Circuit Modeling

Extraction Results for an PMOS Transistor with $W = 0.32\mu m$ and $L = 0.18\mu m$

Output:

![Graph showing IDS vs. VDS for PMOS with W=0.32μm, L=0.18μm, and T=25°C](image)
Circuit Modeling

SEC. 3.11 - SUMMARY

- Model philosophy for analog IC design
  Use simple models for design and sophisticated models for verification
- Models have several parts
  Large signal static (dc variables)
  Small signal static (midband gains, resistances)
  Small signal dynamic (frequency response, noise)
  Large signal dynamic (slew rate)
- In addition models may include:
  Temperature
  Noise
  Process variations (Monte Carlo methods)
- Computer models
  Must be numerically efficient
  Quickly derived from new technology
- Analog Design “Tricks”
  Stay away from minimum channel length if possible
  - Larger $r_{ds}$ → larger gains
  - Better agreement
  Don’t use the computer models for design, rather verification of design